## REMARKS

Applicant appreciates the detailed examination evidenced by the Official Action dated February 6, 2002 (hereinafter "the Official Action"). Applicant has amended Claims 36, 37, and 39 in view of the rejections under 35 USC § 112, second paragraph, to advance the prosecution of the case, despite Applicant's belief that the these claims, as filed, complied with 35 USC § 112, second paragraph.

Applicant maintains that all claims are patentable over Sato, as Sato does not disclose, among other things, the recitations of independent Claim 35 which recites in-part:

> forming a dielectric layer on an integrated circuit substrate, the dielectric layer including a closed via therein that encloses an inner portion of the dielectric layer, and is enclosed by an outer portion of the dielectric layer; and
>
> forming a conductive pattern in the closed via and on the dielectric layer opposite the substrate.

In particular, as understood by Applicant, Sato discusses formation of **conductors in an electrode layer**. *Sato, col. 4, line 53 to col. 5 line 1.* Therefore, Sato does not disclose "forming **a dielectric layer** on an integrated circuit substrate, **the dielectric layer including a closed via therein that encloses an inner portion of the dielectric layer, and is enclosed by an outer portion of the dielectric layer**."

Applicant has also added a new independent Claim 40 and new dependent Claims 41 which are also patentable over Sato. Accordingly, Applicant respectfully requests the withdrawal of all rejections and the allowance of all claims for at least the reasons discussed herein.

**The claims comply with 35 USC § 112, second paragraph**

Dependent Claims 36, 37, and 39 stand rejected under 35 USC § 112, second paragraph over various recitations therein referring to steps of independent Claim 35 that are further defined in those dependent claims. *Official Action, pages 3-4.* As indicated above, Applicant believes that the claims, as filed, comply with 35 USC § 112, second paragraph as the recitations that were rejected are provided in the claims

to clearly identify which steps are to be further defined by the respective dependent claim.

However, Applicant has amended Claims 36, 37, and 39 the recitations therein which refer to a particular step in independent Claim 35 as suggested/interpreted by the Examiner. For example, dependent Claim 36 has been amended to recite that "wherein the step of forming the conductive pattern comprises **the** step of forming a conductive pattern filling the closed via and on the dielectric layer opposite the substrate."

Applicant has also amended Claim 37 to recite "forming the dielectric layer and forming the conductive pattern are repeatedly and sequentially performed to form a multilayer bonding pad" to further clarify that the dielectric layer and the conductive pattern are formed in pairs.

Applicant point outs, however, that these claims have not been amended for reasons related to patentablity as these amendments make explicit what was already implied in the original claim language. Applicant respectfully requests withdrawal of the rejections under 35 USC § 112, second paragraph.

**Independent Claim 35 is patentable over Sato**

Claims 35-39 stand rejected under 35 USC § 102(e) over U.S. Patent No. 5,739,587 to Sato ("Sato"). *Official Action, pages 4-5.* Applicant respectfully traverses the rejections as Sato does not disclose all of the recitations of the claims as required under section 102.

The Official Action appears to argue that Sato Figures 3, 8, and 11 disclose the recitation of "forming a dielectric layer on an integrated circuit substrate, the dielectric layer including a closed via therein that encloses an inner portion of the dielectric layer, and is enclosed by an outer portion of the dielectric layer," as recited in independent Claim 35. *Official Action, page 4.* Respectfully, the cited figures of Sato do not disclose what the Official Action alleges. For example, Figure 8 shows an upper electrode layer 100 having concentric grooves therein. Conductors 102, 103, and 104 are formed in the concentric grooves. *Sato, col. 4, line 54 and col. 6, lines 36-40.* Therefore, as understood by Applicant, Figure 8 shows conductors 102, 103,

and 104 in the upper electrode plate. Even assuming for the sake of argument that the conductors in Sato could be considered vias as recited in the claims, the conductors in Sato are not included in a **dielectric** layer. Moreover, the conductors in Sato, in contrast to the recitations of the claim, do not **enclose an inner portion of the dielectric layer, and [are not] enclosed by an outer portion of the dielectric layer**.

Figure 3 of Sato also does not disclose the recitations of the claims. The insulating film 60 shown in Figure 3 of Sato, argued to disclose the dielectric layer recited in the claims, **does not include a closed via therein that encloses an inner portion of the dielectric layer, and is enclosed by an outer portion of the dielectric layer**. Actually, as understood Applicant, the vias 41-44 shown in Figure 3 of Sato are solid and, therefore, do not appear to enclose any of the insulating film 60. Furthermore, Figure 11 of Sato appears to show a structure similar to that shown in Figure 3 and, therefore, also does not disclose the recitations of independent Claim 35.

Independent Claim 35 is patentable over Sato for at least the reasons discussed above. Furthermore, dependent Claims 36-39 are patentable at least per the patentablity of independent Claim 35.

**Many of the dependent Claims are separately patentable over Sato**

In addition to the reasons discussed above in reference to independent Claim 35, many of the dependent claims provide separate bases for patentability of Sato. For example, Sato does not disclose that "the closed via is at least one of a circular, elliptical, and polygonal via" as recited in dependent Claim 38." Contrary to assertions in the Official Action, Figure 3, 8, and 11 do not disclose these recitations.

As recited in independent Claim 35, the via "encloses an inner portion of the dielectric layer, and is enclosed by an outer portion of the dielectric layer." Therefore, according to dependent Claim 38, the (circular, elliptical, polygonal) via recited in independent claim 35 encloses an inner portion of the dielectric layer, and is enclosed by an outer portion of the dielectric layer. As discussed above in reference to independent Claim 35, Figure 8 of Sato shows concentric conductors 102-104 in grooves **in an electrode layer**. Therefore, as understood by Applicant, the concentric

conductors 102-104 in Figure 8 of Sato do not enclose an inner portion of the **dielectric layer**, and are not enclosed by an outer portion of **the dielectric layer**. Figures 3 and 11 of Sato also do not disclose these recitations. Accordingly, Claim 38 is patentable over Sato for at least these additional reasons.

**New claims 40 and 41 are patentable over Sato**

Applicant has added new independent Claim 40 which recites in-part:

> forming a dielectric layer on an integrated circuit substrate, **the dielectric layer including a closed via therein that encloses an inner portion of the dielectric layer, and is enclosed by an outer portion of the dielectric layer**, **wherein the closed via penetrates the dielectric layer and extends towards the integrated circuit substrate**; and
> forming a conductive pattern in the closed via and on the dielectric layer opposite the substrate.

As discussed above, Sato does not disclose a **dielectric layer including a closed via therein that encloses an inner portion of the dielectric layer, and is enclosed by an outer portion of the dielectric layer**. Sato also does not disclose that a **closed via penetrates the dielectric layer and extends towards the integrated circuit substrate**. For example, as understood by Applicant, Figure 8 of Sato does not show that conductors 102-104 in grooves in electrode 100 penetrate the electrode 100 and extend towards the substrate 10. Accordingly, new Claim 40 is patentable over Sato. Applicant has also added new dependent Claim 41 which recites in-part that "**the conductive pattern penetrates the dielectric layer and extends towards the integrated circuit substrate**." Dependent Claim 41 is patentable over Sato for at least the reasons discussed above in reference to new independent Claim 40.

## CONCLUSION

Applicant has amended Claims 36, 37, and 39 as suggested by the Examiner. Applicant have also shown how Sato does not disclose the recitations of the pending claims. Accordingly, Applicant respectfully requests the withdrawal of all rejections

and the allowance of all claims in due course. If any informal matters arise the Examiner is encouraged to contact the undersigned by telephone at (919) 854-1400.

Respectfully submitted,

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**CERTIFICATE OF MAILING**

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: BOX NON-FEE AMENDMENT, Commissioner for Patents, Washington, DC 20231, on April 5, 2002.

Audra Wooten
Date of Signature: April 5, 2002

## VERSION WITH MARKINGS TO SHOW CHANGES MADE

Sir:

The following is an addendum to the concurrently filed amendment in response to an Official Action dated February 6, 2002 in the above referenced application. This addendum includes a marked-up version of the changes made to the claims by the present amendment.

**In the Claims:**

Claims 36, 37 and 39 have been amended as follows:

36. (Amended) A method according to Claim 35 wherein the step of forming [a] the conductive pattern comprises the step of forming a conductive pattern filling the closed via and on the dielectric layer opposite the substrate.

37. (Amended) A method according to Claim 35 wherein the steps of forming [a] the dielectric layer and forming [a] the conductive pattern are repeatedly and sequentially performed to form a multilayer bonding pad on the integrated circuit substrate.

39. (Amended) A method according to Claim 35:

wherein the step of forming [a] the dielectric layer comprises the step of forming a dielectric layer on an integrated circuit substrate, the dielectric layer including the closed via and an open via therein; and

wherein the step of forming [a] the conductive pattern comprises the step of forming a conductive pattern in the closed via, in the open via and on the dielectric layer opposite the substrate.

The following new Claims 40 and 41 have been added:

40. (New) A method of forming bonding pad for an integrated circuit comprising the steps of:

forming a dielectric layer on an integrated circuit substrate, the dielectric layer including a closed via therein that encloses an inner portion of the dielectric layer, and is enclosed by an outer portion of the dielectric layer, wherein the closed via penetrates the dielectric layer and extends towards the integrated circuit substrate; and

forming a conductive pattern in the closed via and on the dielectric layer opposite the substrate.

41. (New) A method according to Claim 40 wherein the step of forming the conductive pattern comprises forming the conductive pattern in the closed via and on the dielectric layer opposite the substrate, wherein the conductive pattern penetrates the dielectric layer and extends towards the integrated circuit substrate.

**END**